

Fig. 1

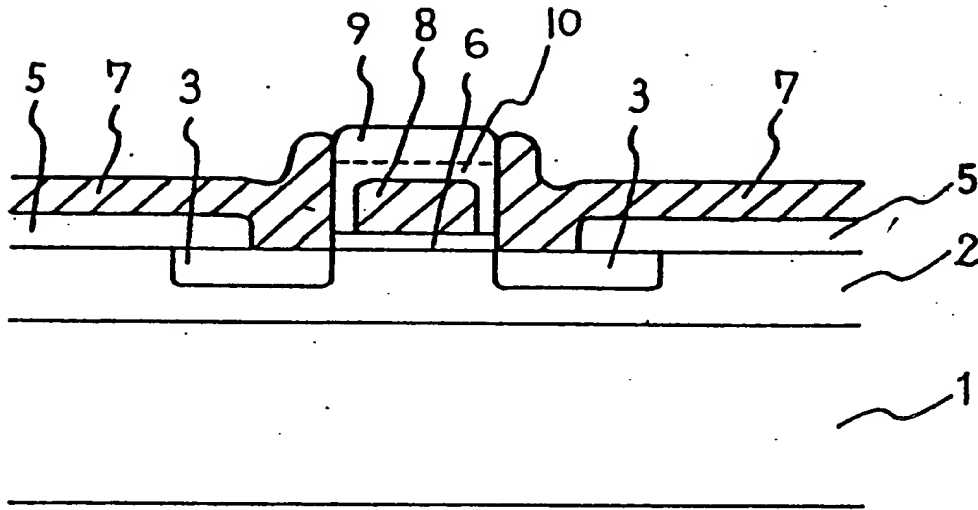


Fig. 2

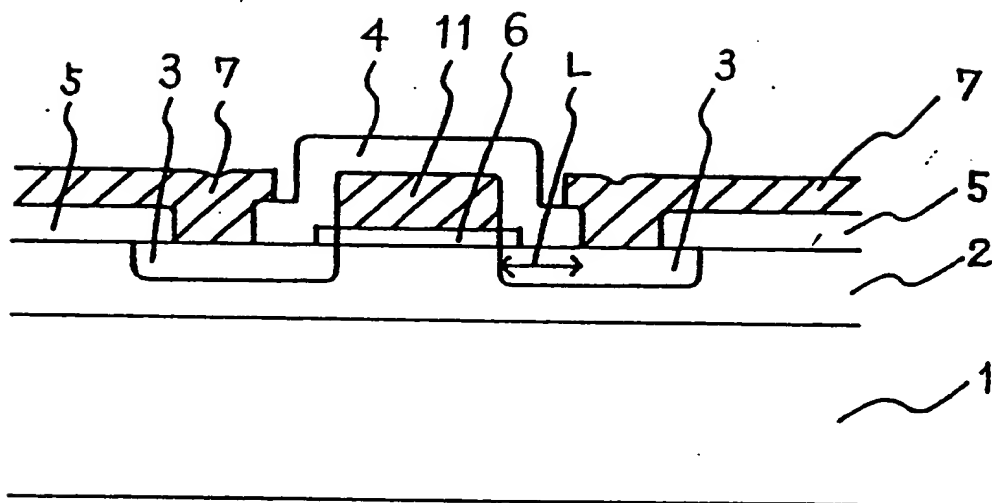


Fig. 3

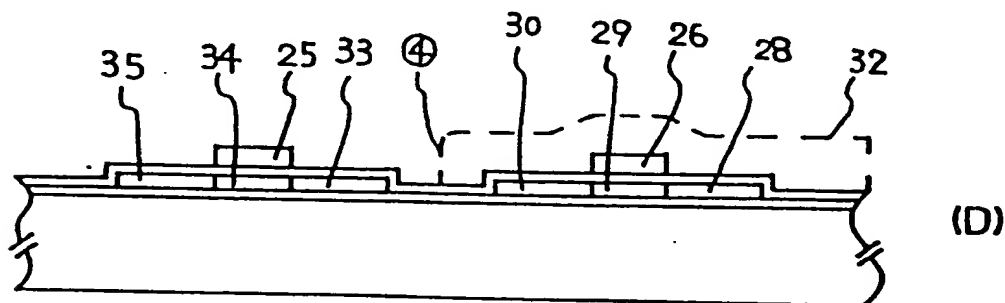
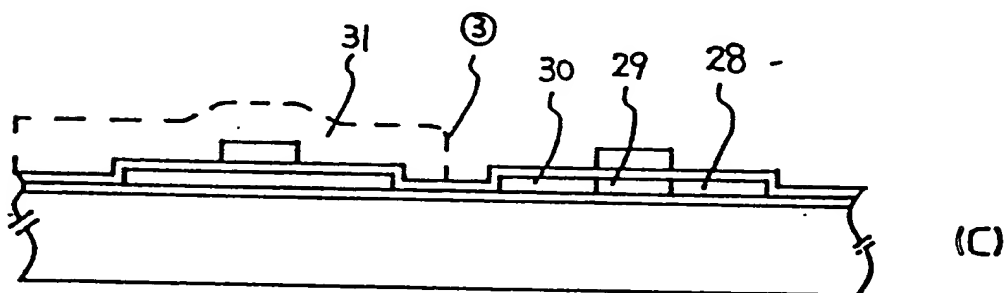
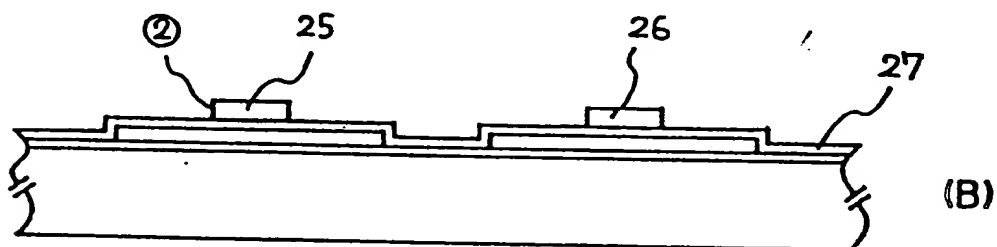
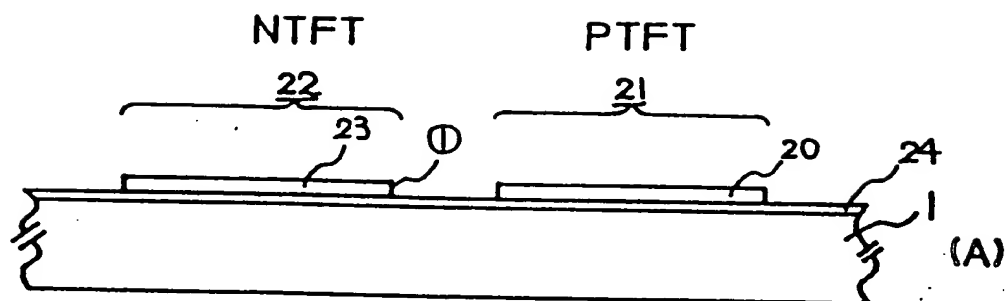
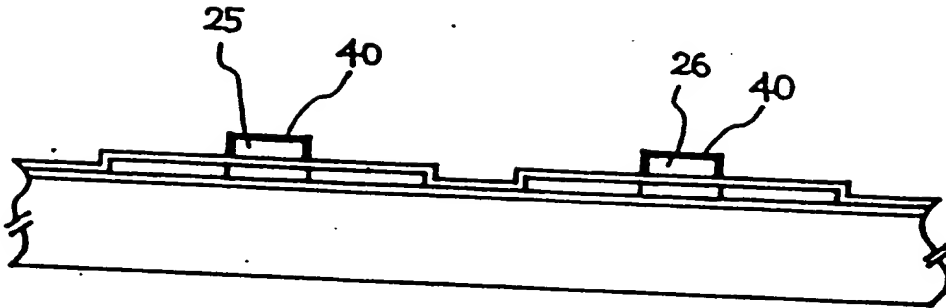
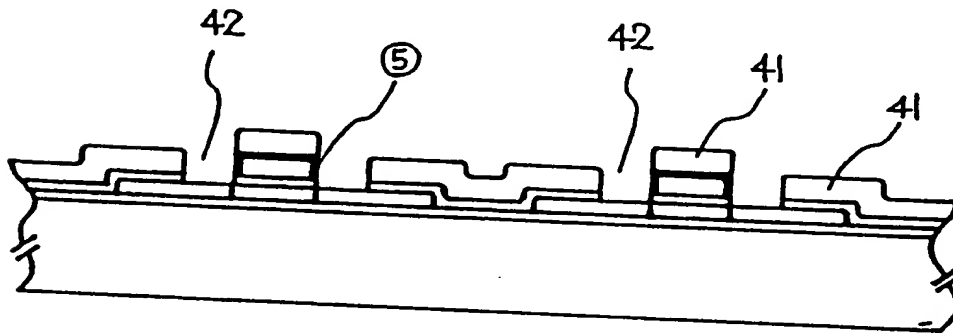


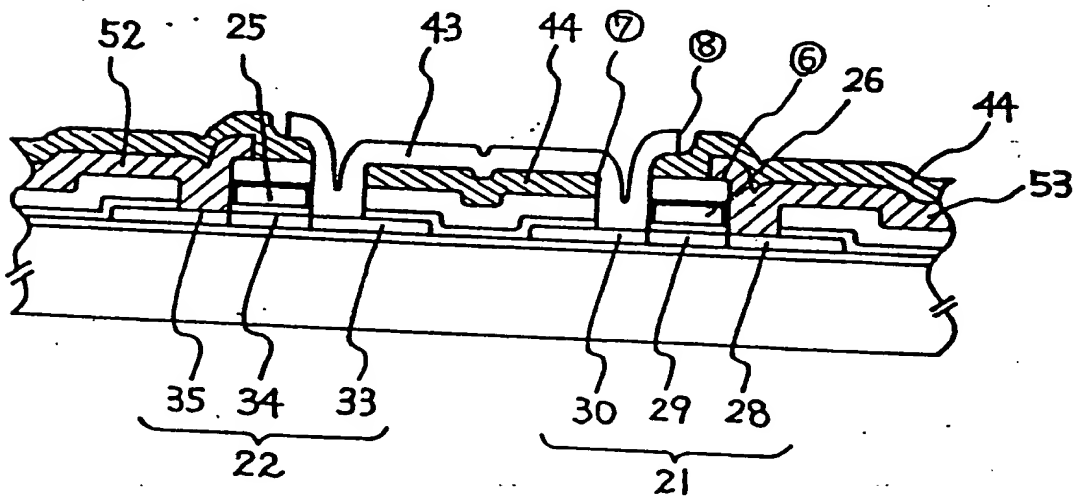
Fig. 3



(E)



(F)



(G)

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Fig. 4

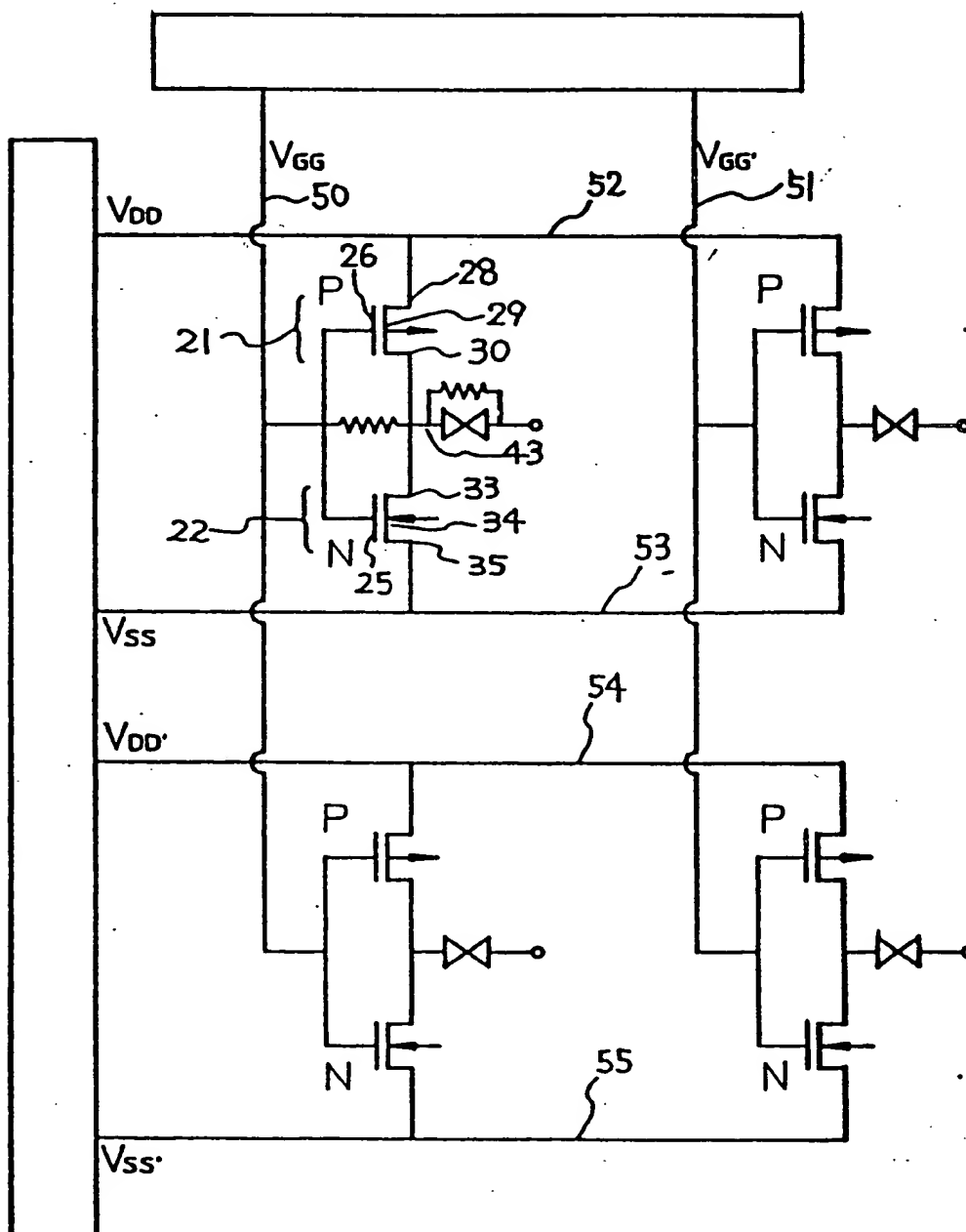
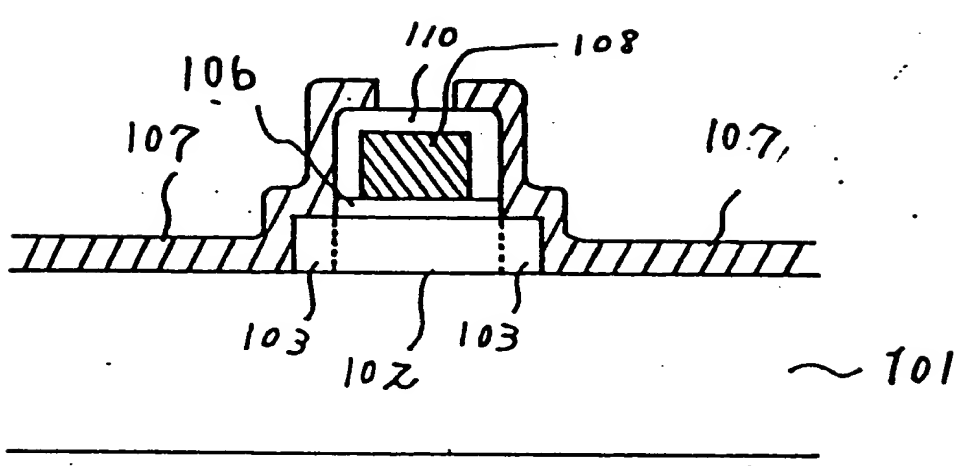


Fig. 5



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Fig. 6

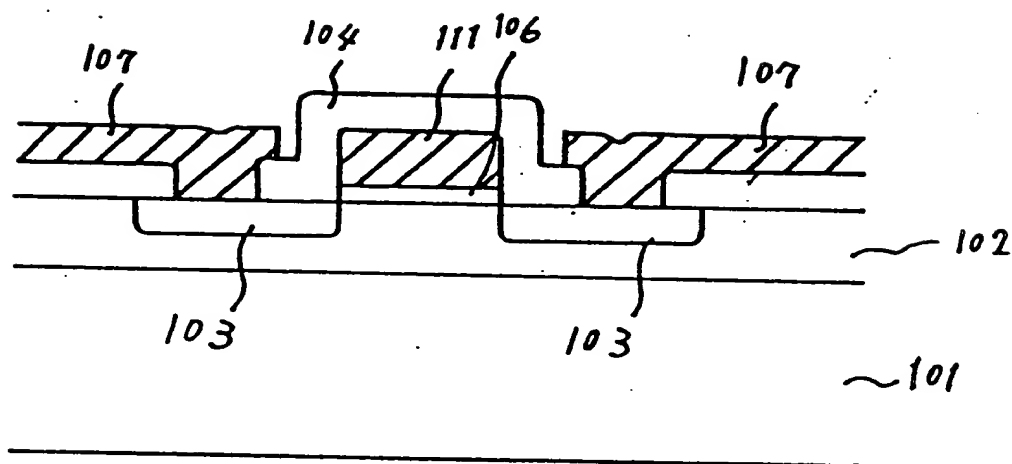
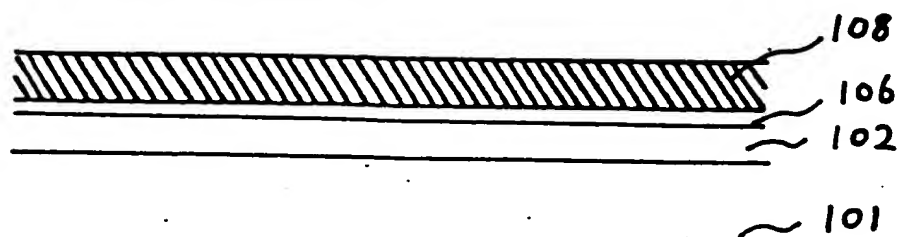
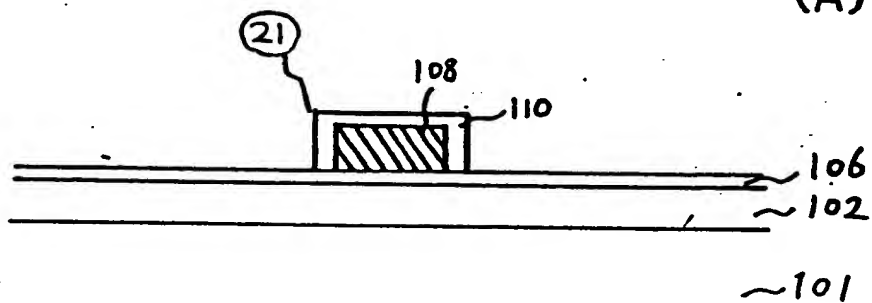


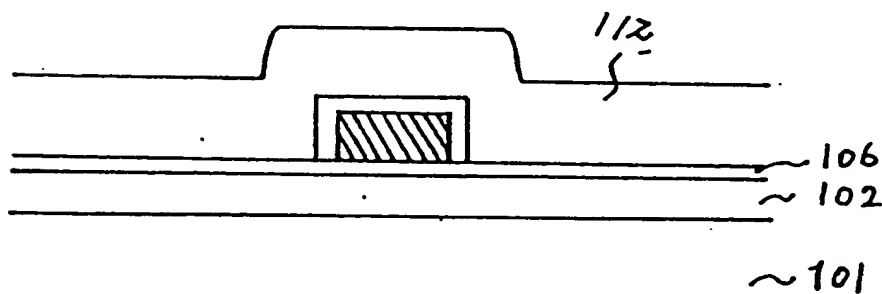
Fig. 7



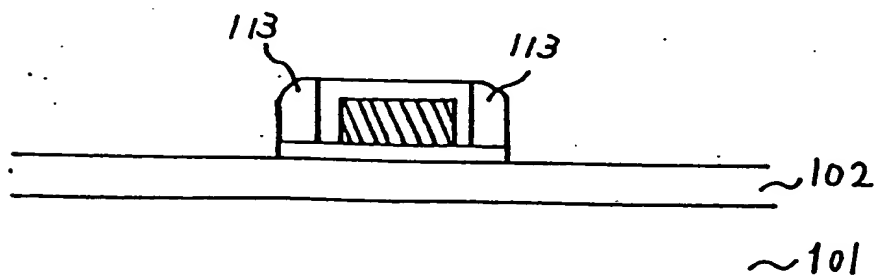
(A)



(B)



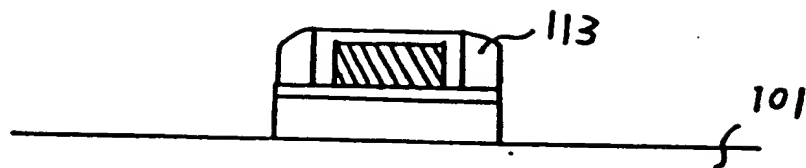
(C)



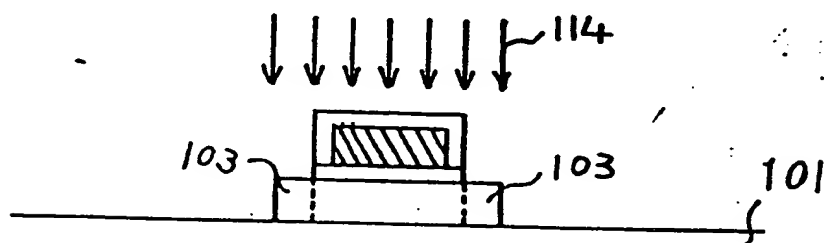
(D)



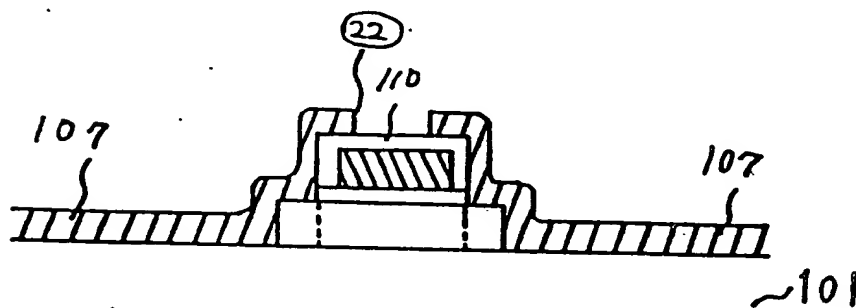
Fig. 7



(E)



(F)



(G)

Fig. 8

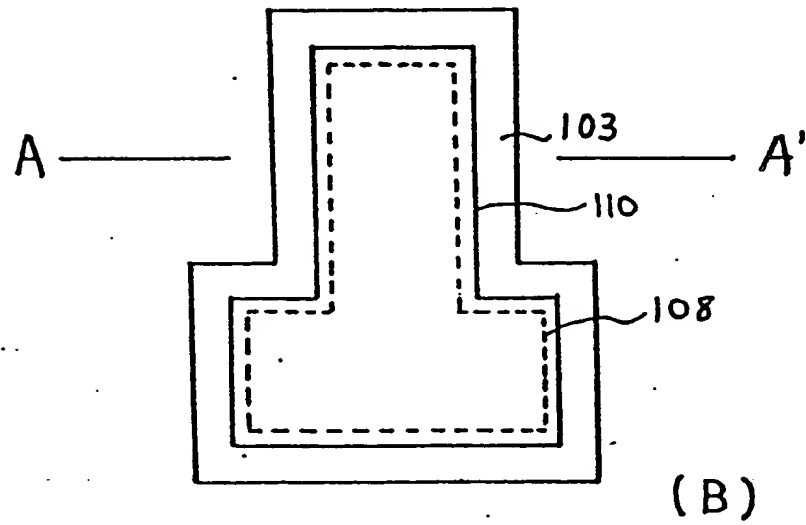
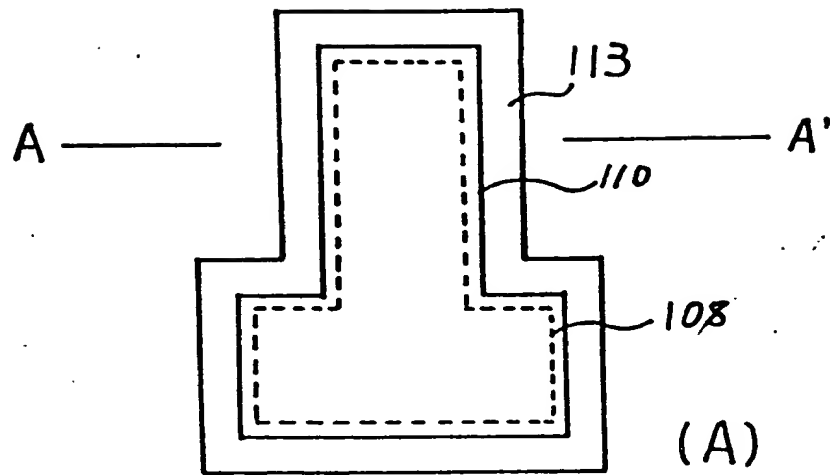


Fig. 8

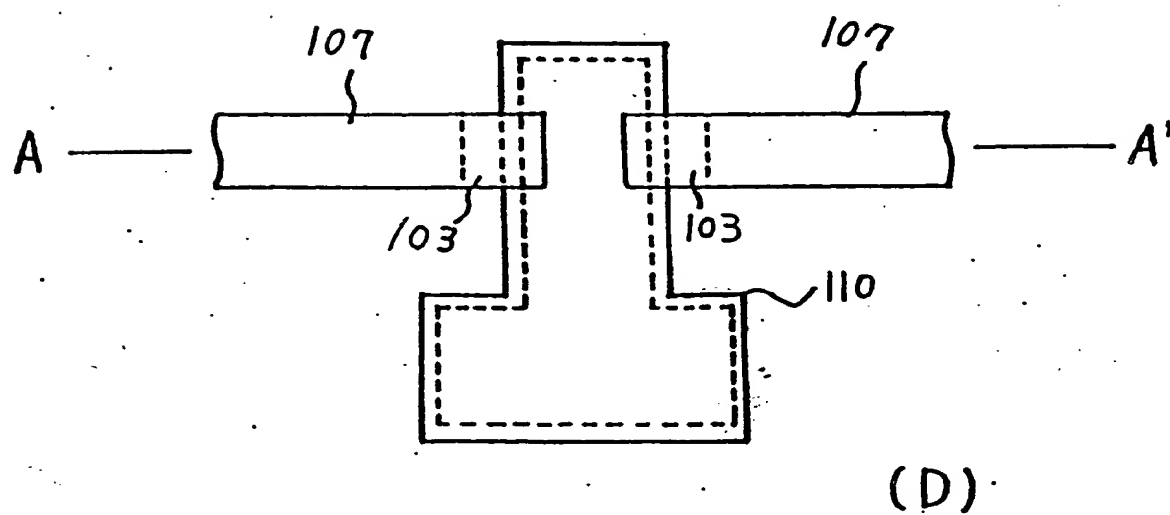
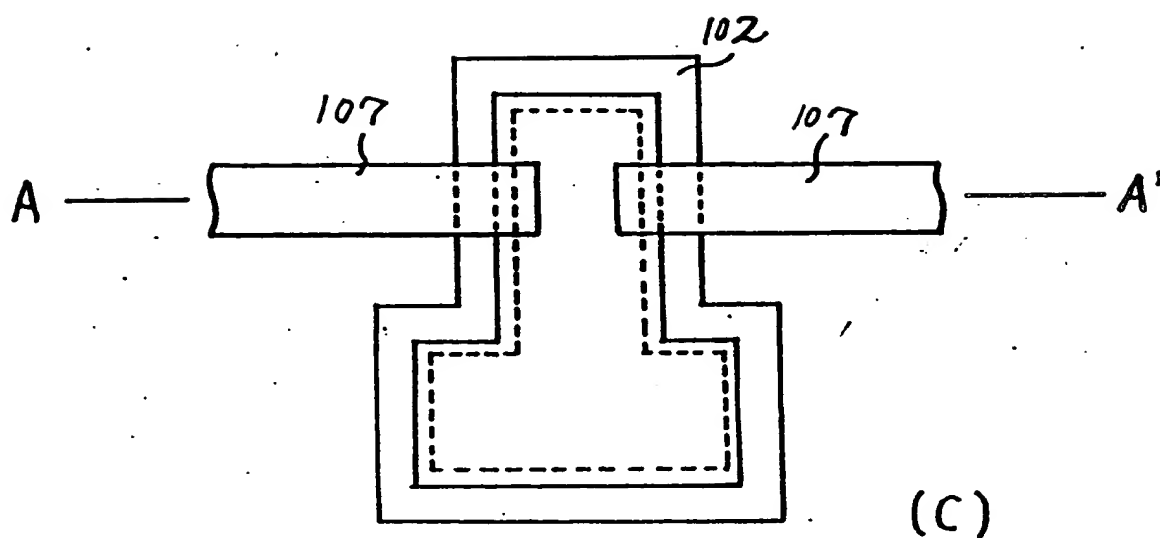
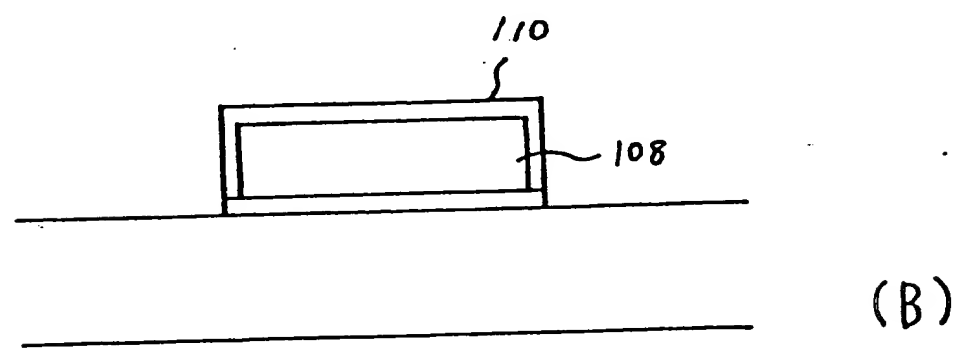
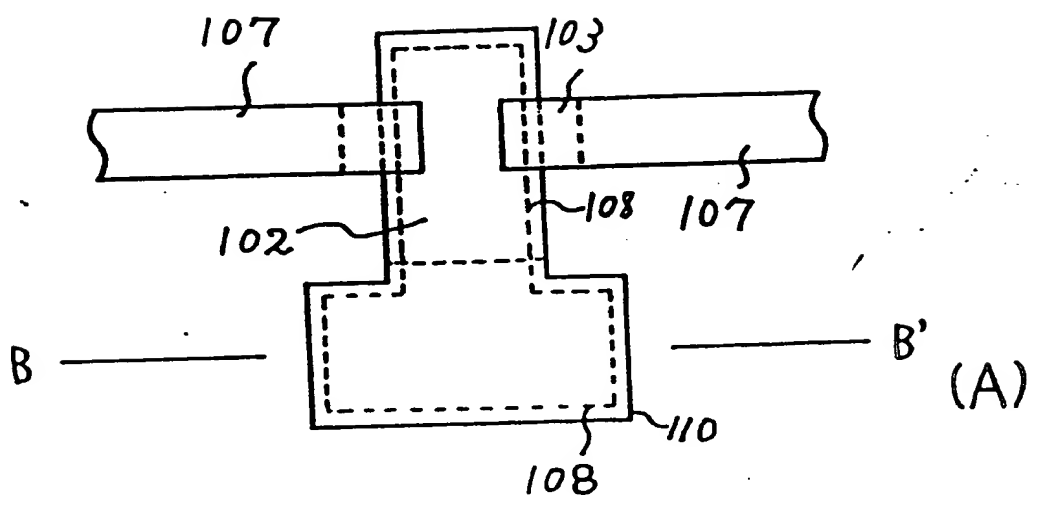


Fig. 9



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The schematic diagram illustrates a semiconductor device 180, which is a cross-sectional view of a multi-layered structure. The device is divided into two main vertical sections, each containing a stack of transistors and diodes. The top section features a P-type transistor 161 (gate 155, drain 156, source 160) and an N-type transistor 162 (gate 156, drain 161, source 162). A diode 160 is connected between the drain of transistor 161 and the source of transistor 162. The bottom section features a P-type transistor 161 (gate 155, drain 156, source 160) and an N-type transistor 162 (gate 156, drain 161, source 162). A diode 160 is connected between the drain of transistor 161 and the source of transistor 162. The device is connected to various power supplies: VDD (172) at the top, VSS (173) at the bottom, VGG (157) on the left, and VGG' (176) on the right. The device is also connected to a common ground (174) and a common supply (175).

Fig. 11

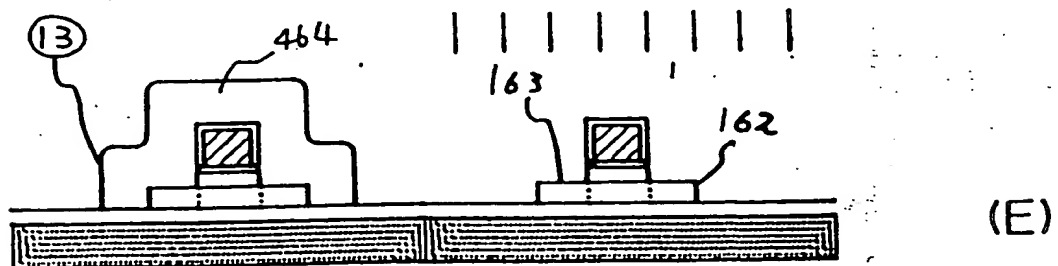
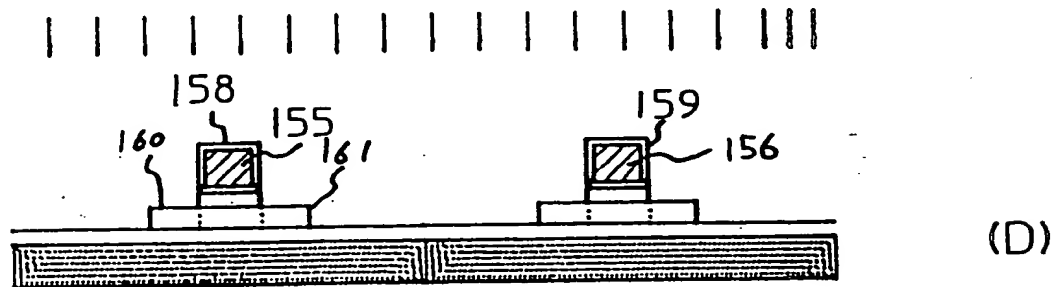
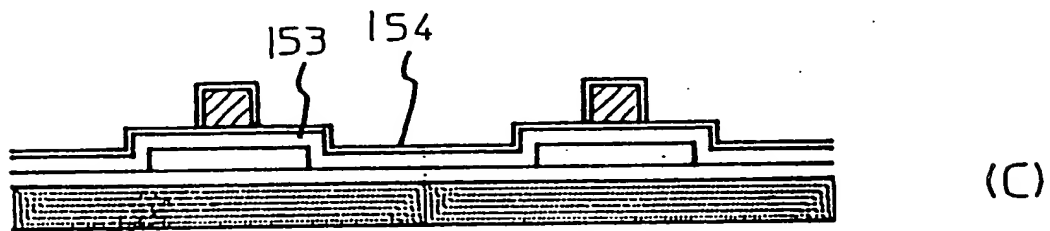
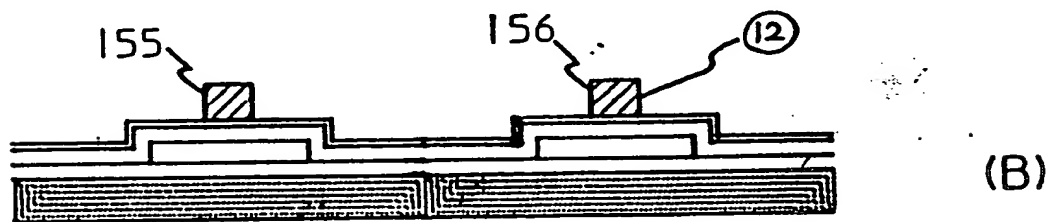
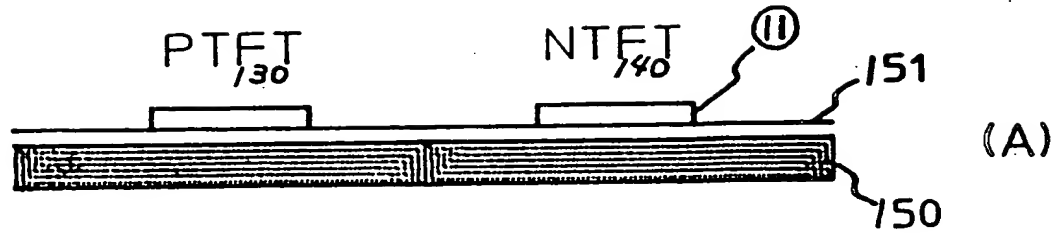
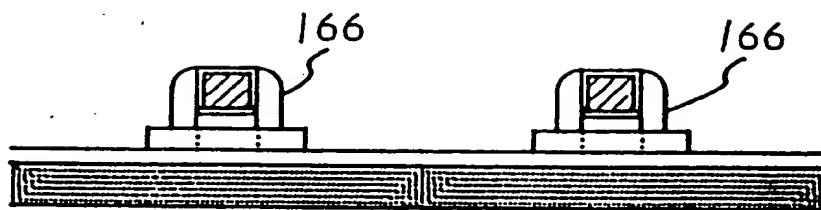
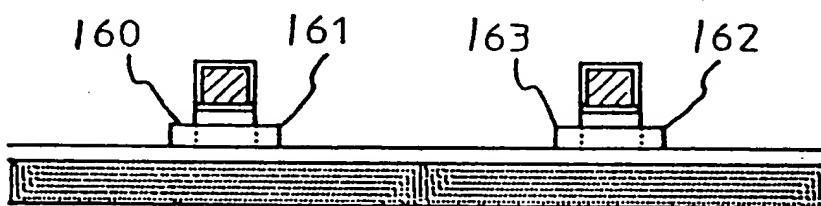


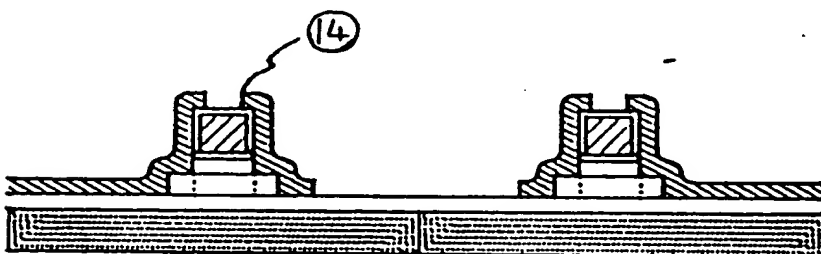
Fig. 11



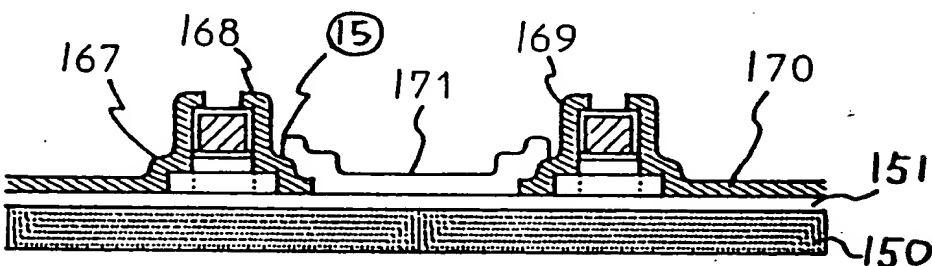
(F)



(G)



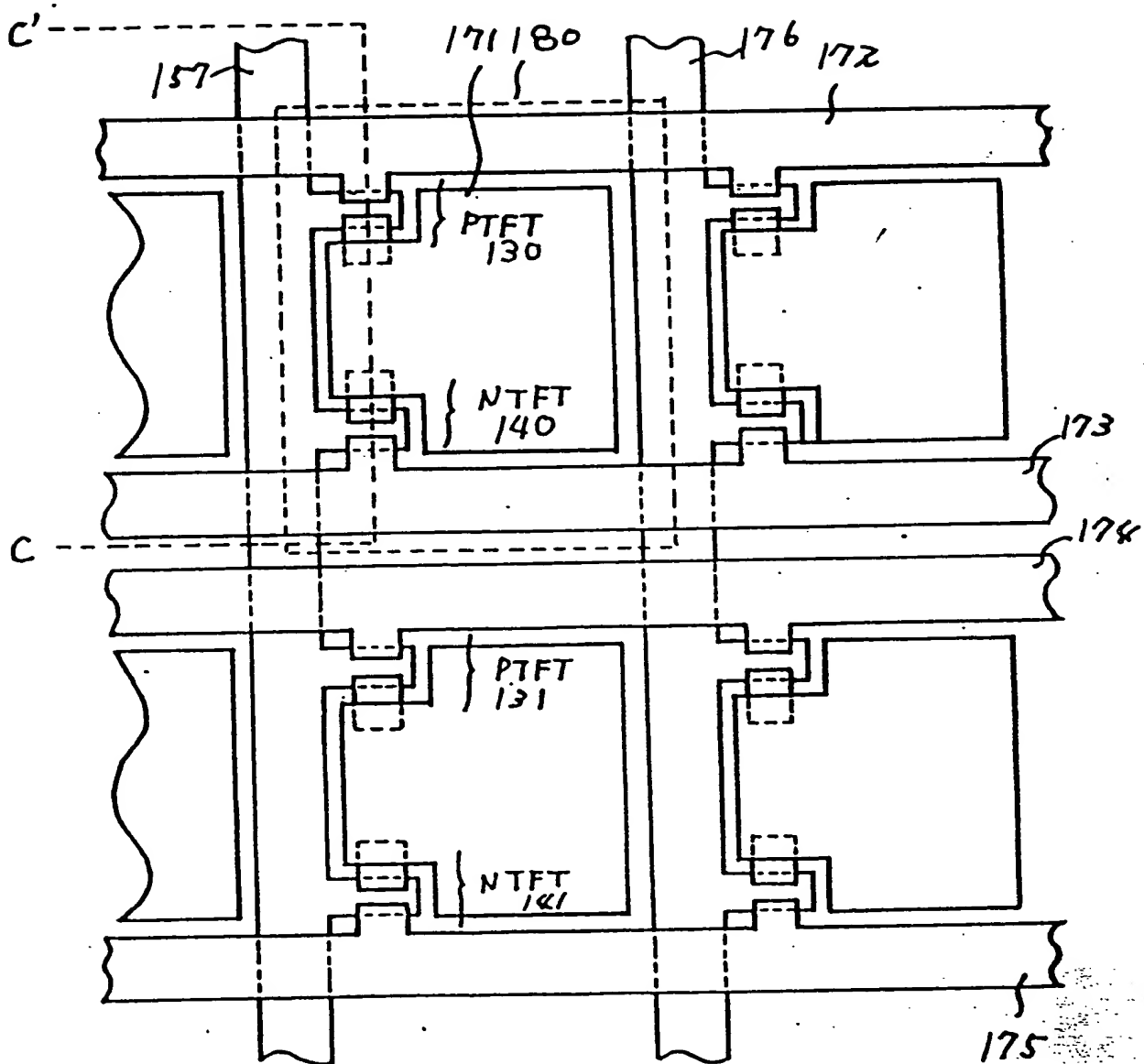
(H)



(I)

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Fig. 12



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Fig. 13

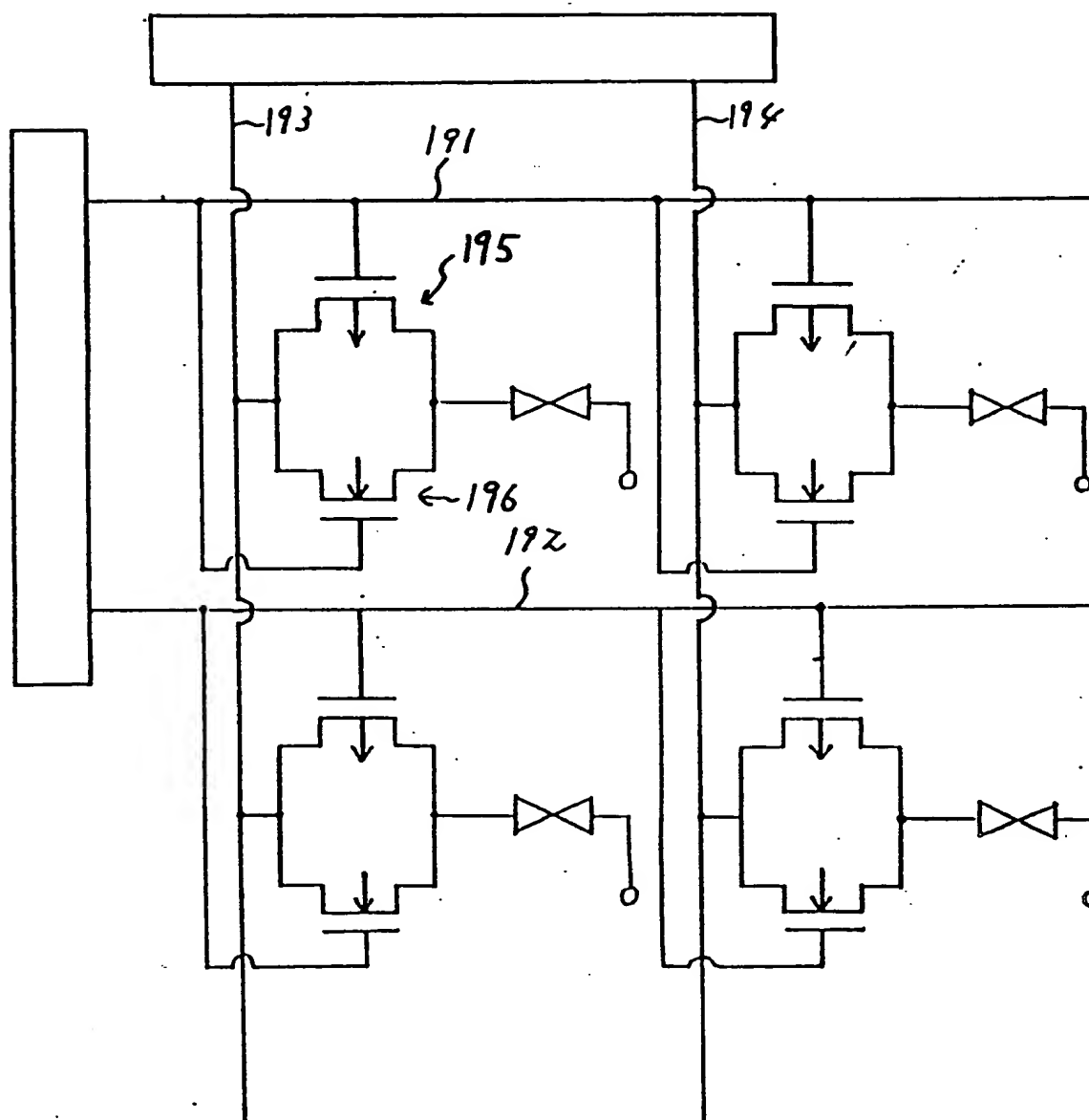


Fig. 14

